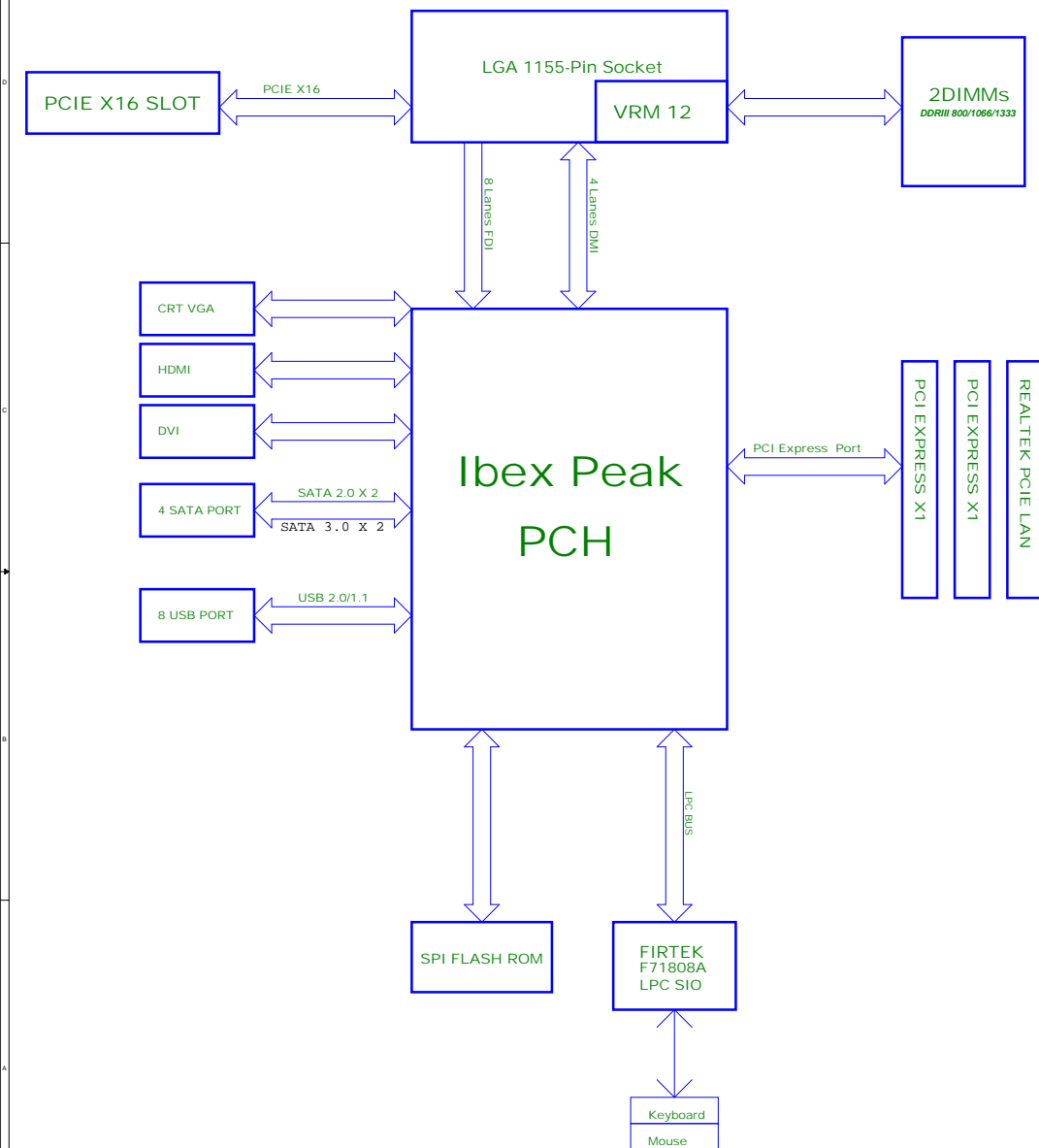


# BLOCK DIAGRAM

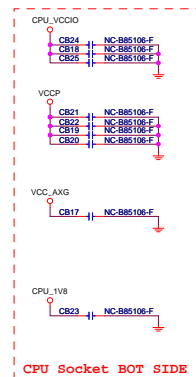
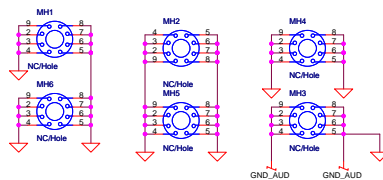
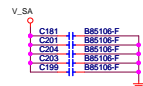
## PAGE TITLE

01. BLOCK DIAGRAM
02. CPU MAIN & PCIE
03. CPU MEMORY & GND
04. CPU POWER
05. DDRIII A
06. DDRIII B
07. PCH MAIN
08. PCH CLOCK & DISPLAY
09. PCH POWER & GND
10. LPC SIO & H/W MONITOR
11. PCI & PCIEX1 SLOT & SDVO SLOT
12. HD AUDIO
13. PCIE X 16 SLOT
14. POWER,USB & FRONT CONN.
15. CLOCK GEN.
16. CPU POWER PWM
17. CPU POWER DRIVER
18. SYSTEM POWER I
19. SYSTEM POWER II
20. RTL8111D/8102EL PCI-E LAN





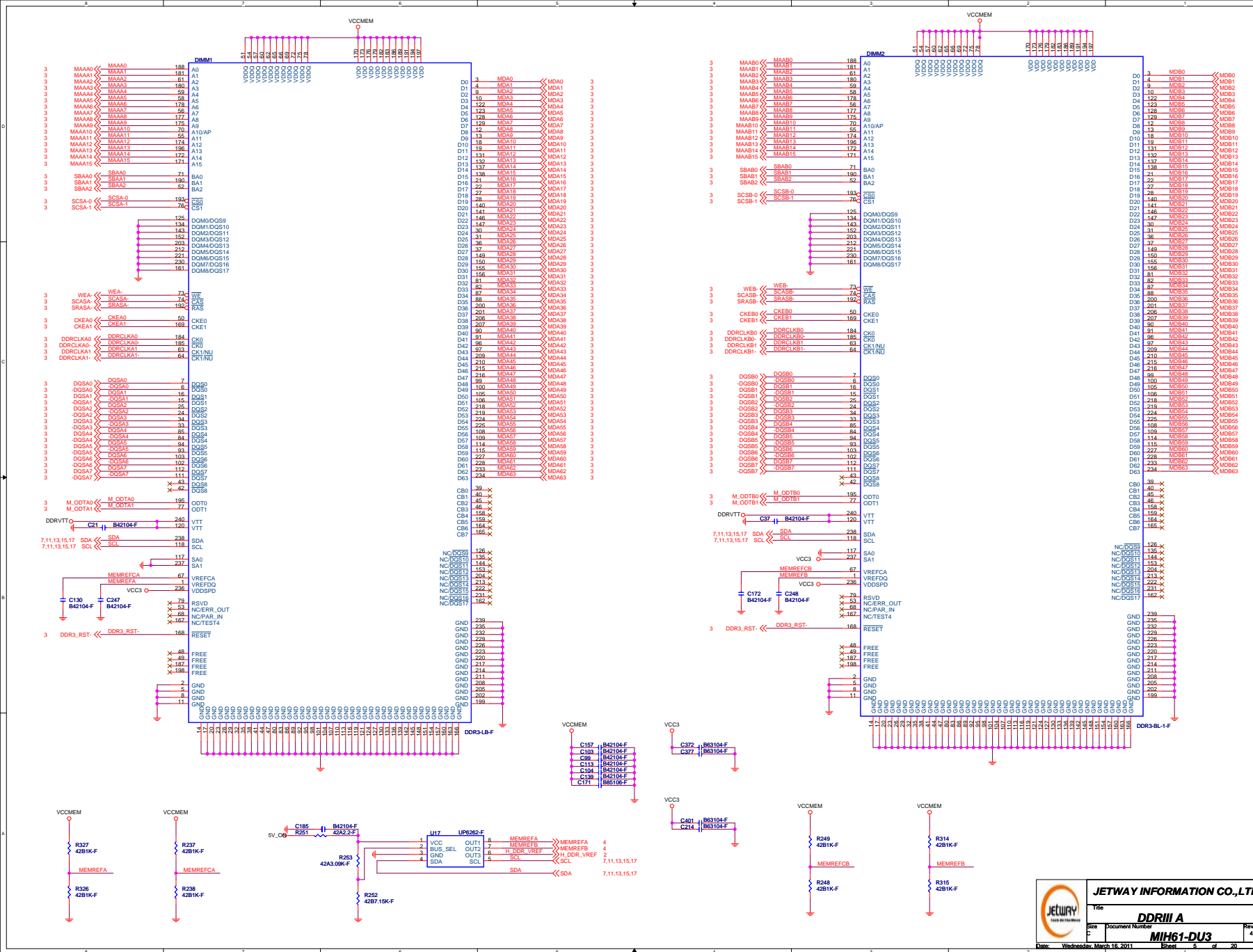


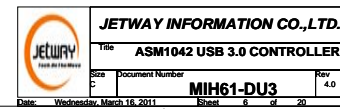


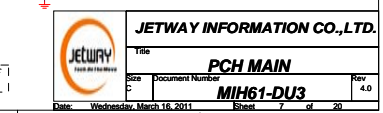
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C	<b>MIH61-DU3</b>

Date: Wednesday, March 16, 201

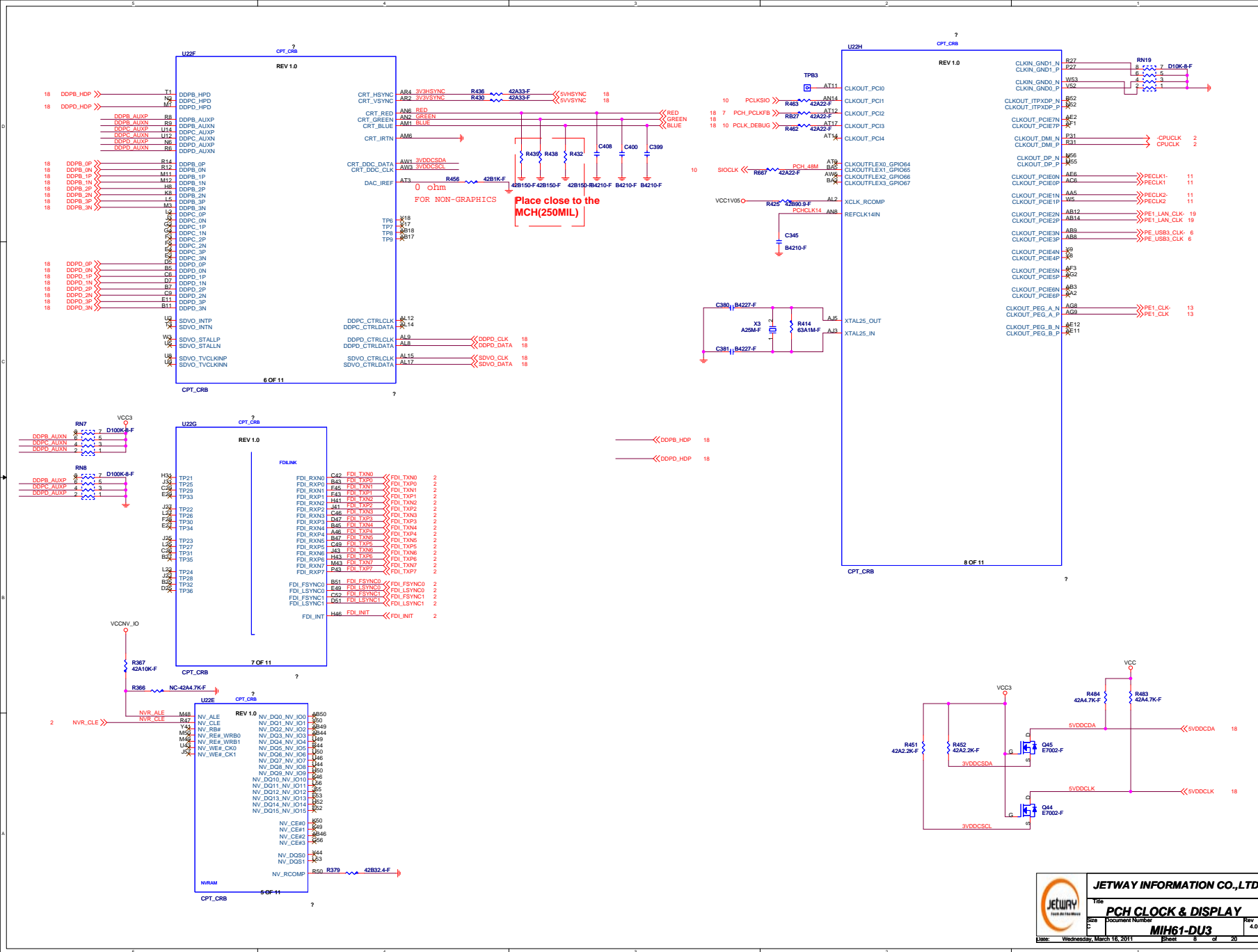
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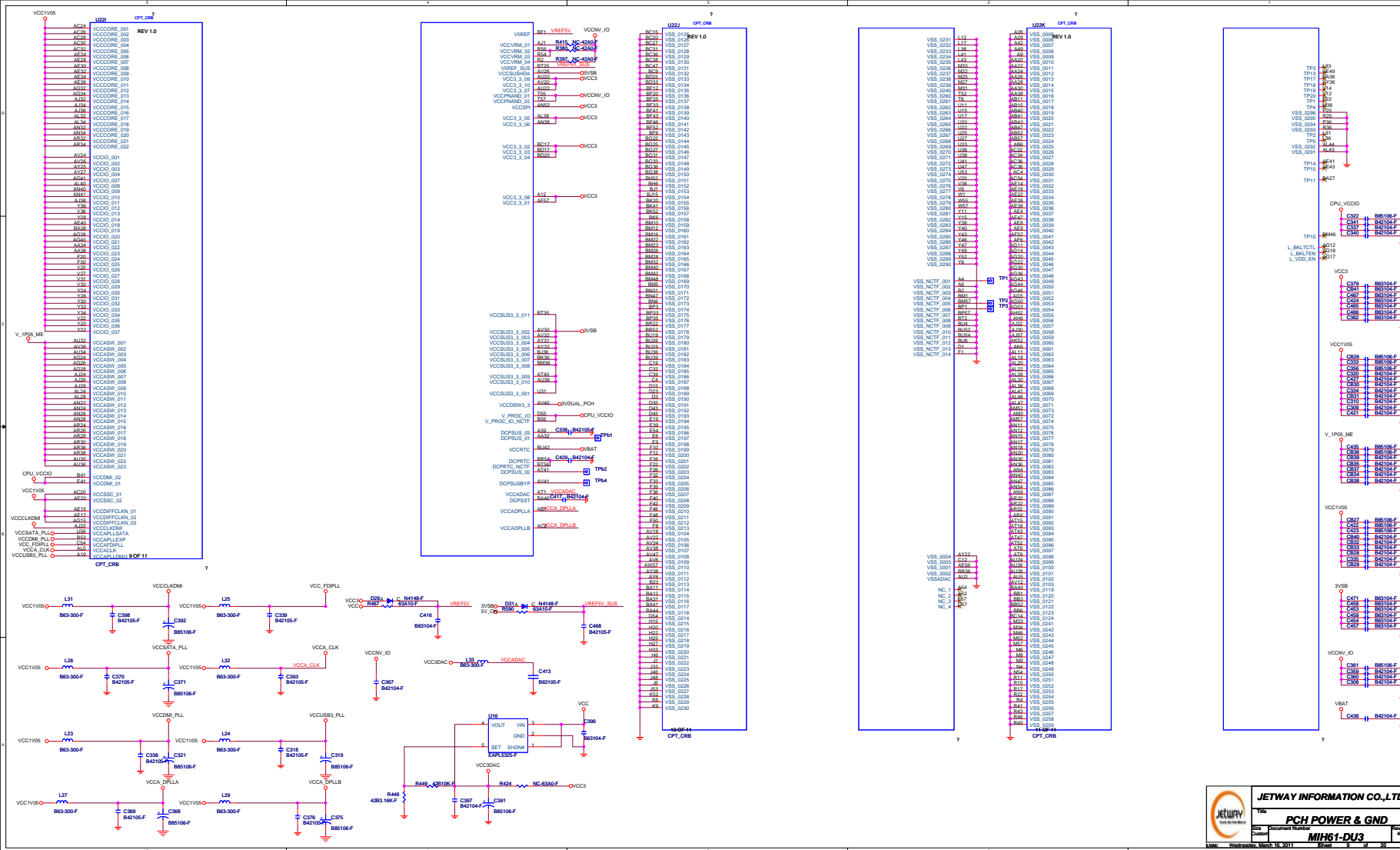












Power On Strapping Options

PIN2 DTR2# HI:SPI as a back up BIOS(Default)  
LO:SPI as primary BIOS

PIN3 RT92# HI:PWM FAN(Default)  
LO:DMC FAN

PIN5 SOUT2 HI:SPI Function Disable.(Default)  
LO:SPI Function Enable.

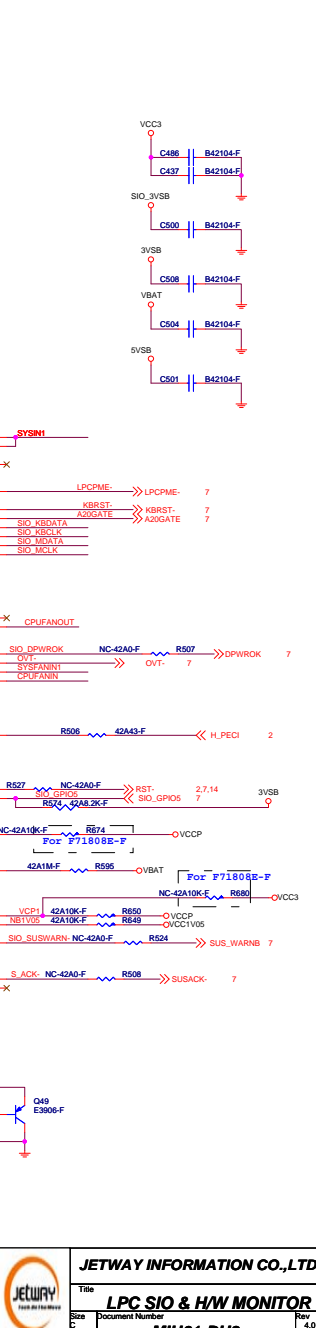
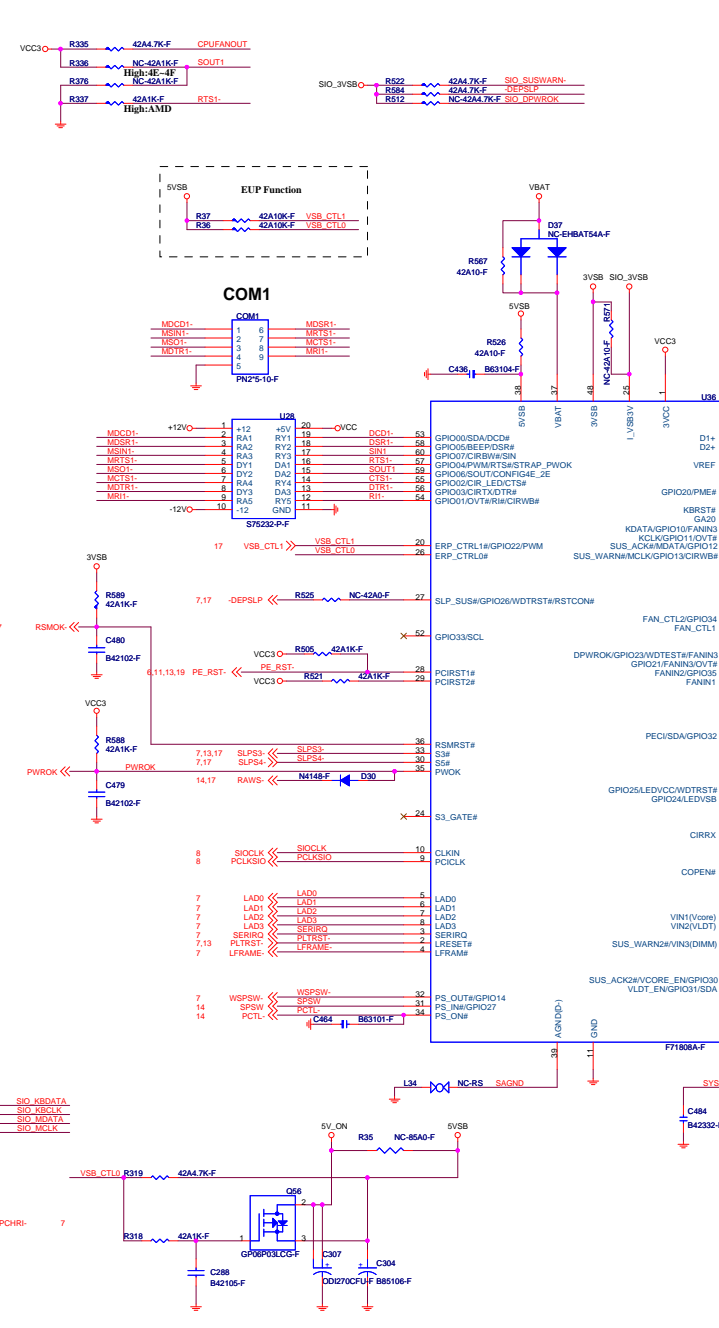
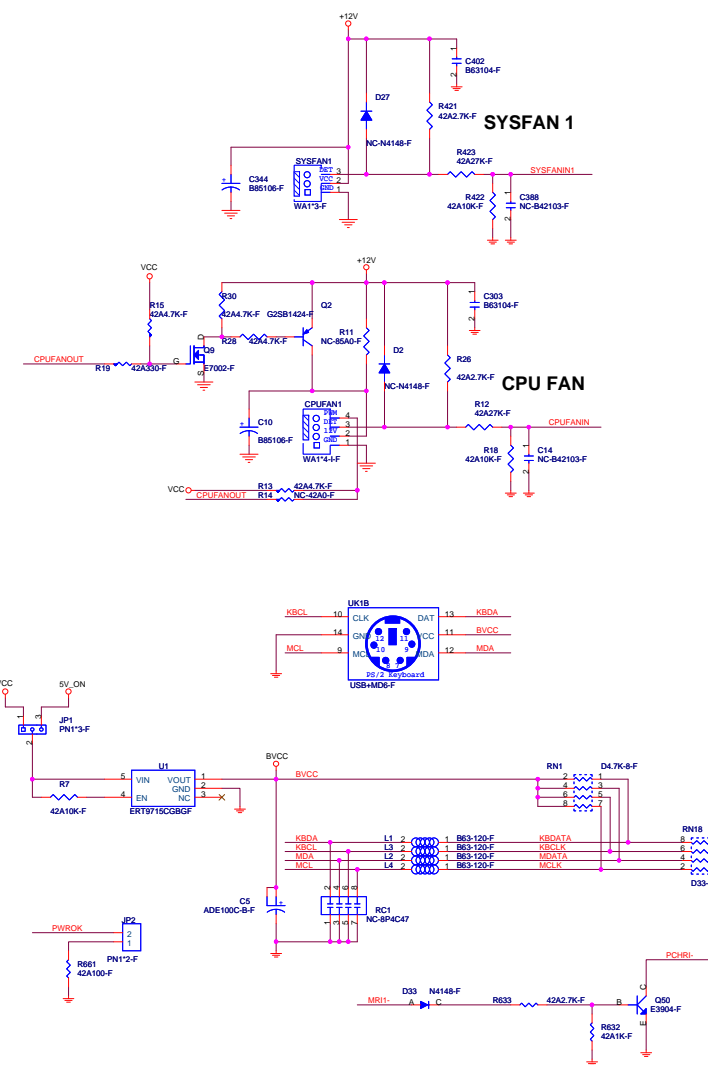
PIN28 LDRQ# HI:PIN 51-56 are bus Interface(Default)  
LO:PIN 51-56 are GPIO pin

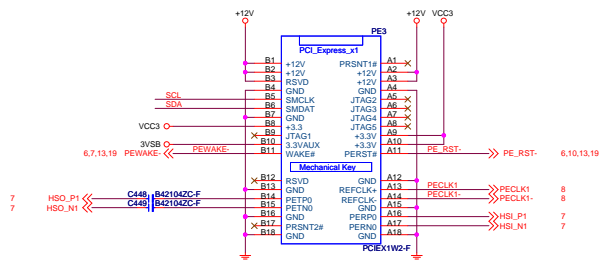
PIN104 SLIN# Pull High 1K Pin 100-116 as LPT Interfaces  
Pull High 20K Pin 100-116 as PVID Controller  
Pull Down 1K Pin 102/103/111/112 as SVID Controller  
Pull Down 47K Pin 100-103 & 105-116 as GPIO Pin

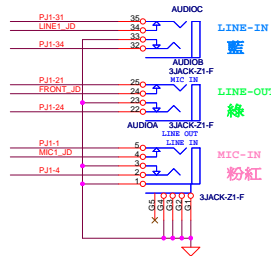
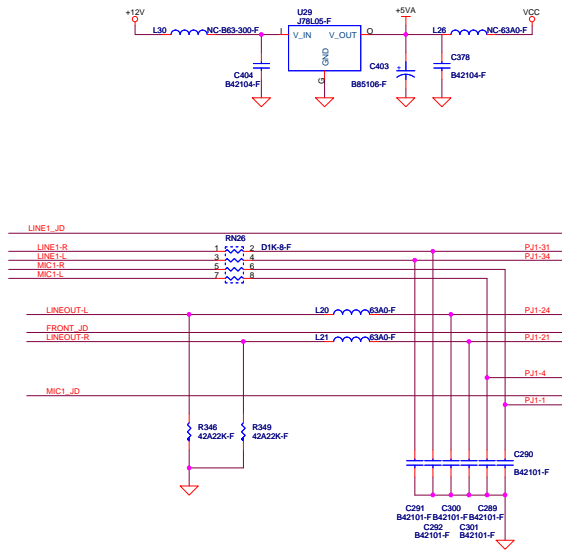
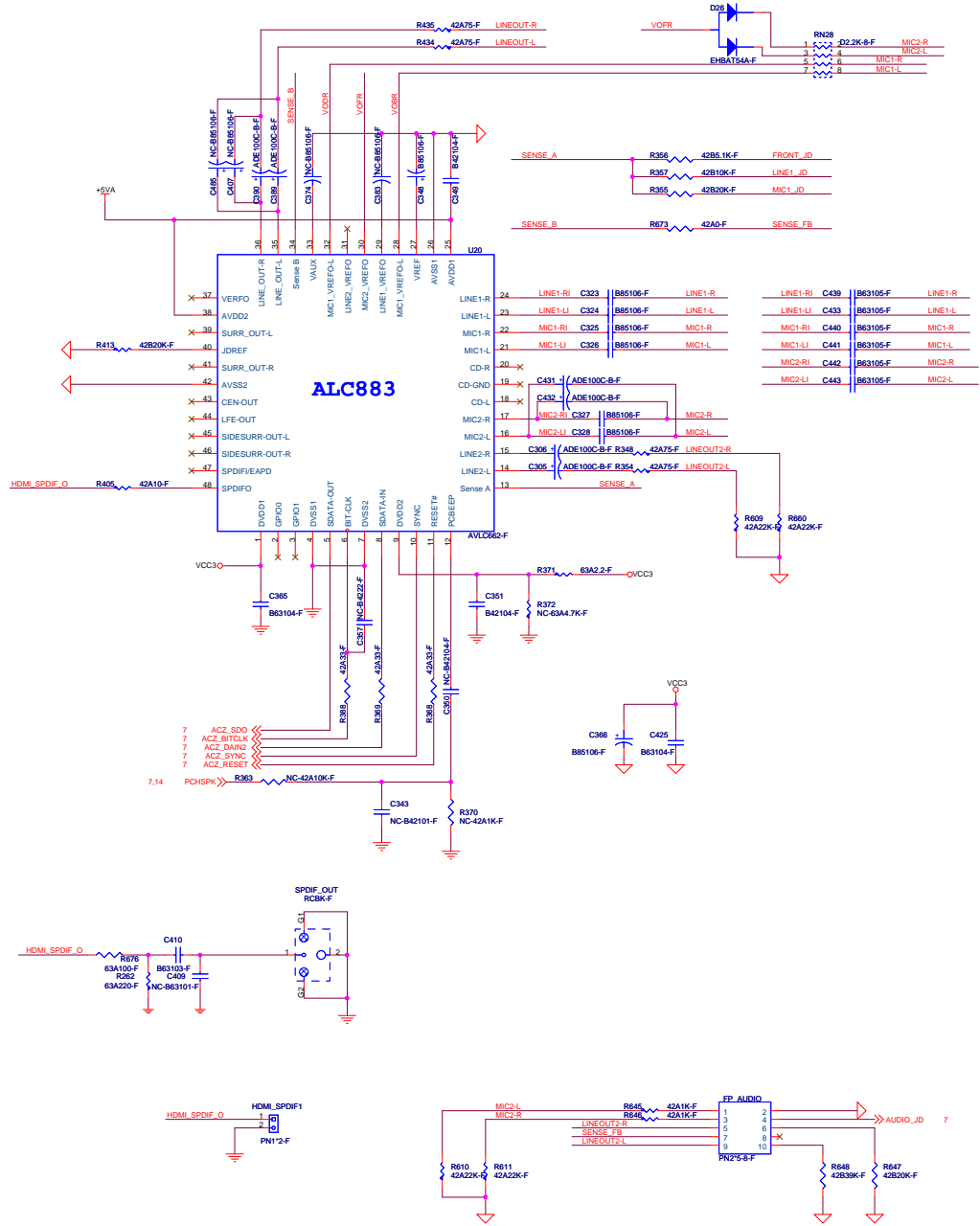
PIN121 DTR1# HI:FAN Default Duty 60%.(Default)  
LO:FAN Default Duty 100%.

PIN122 RTS1# HI:80 port decode output form COM2 Interface (Default)  
LO:Disable the 80 port function.

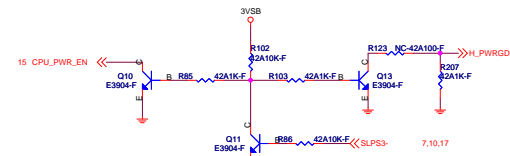
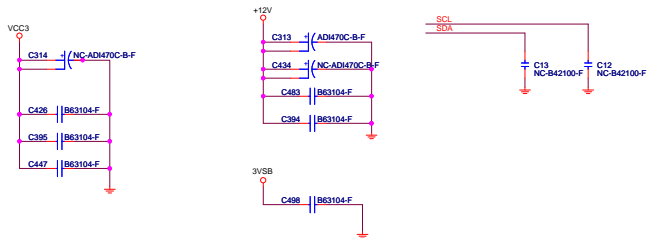
PIN124 SOUT1 HI:4E.(Default)  
LO:2E

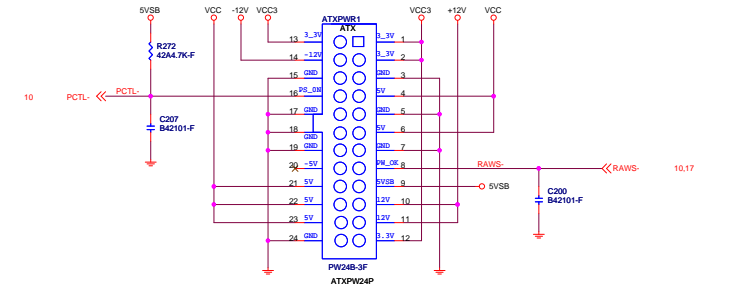
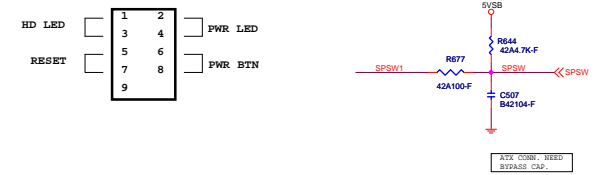
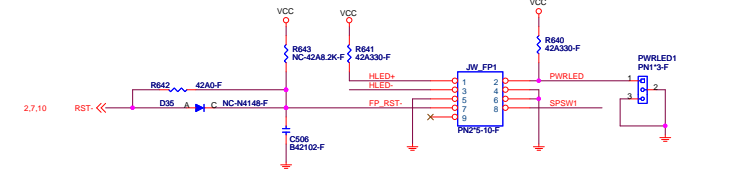
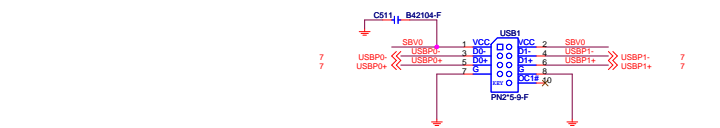
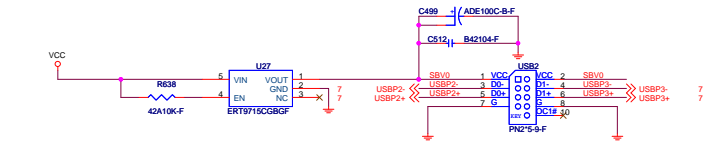
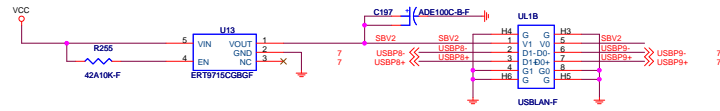
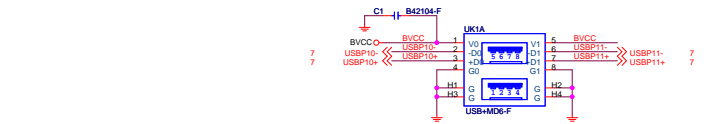


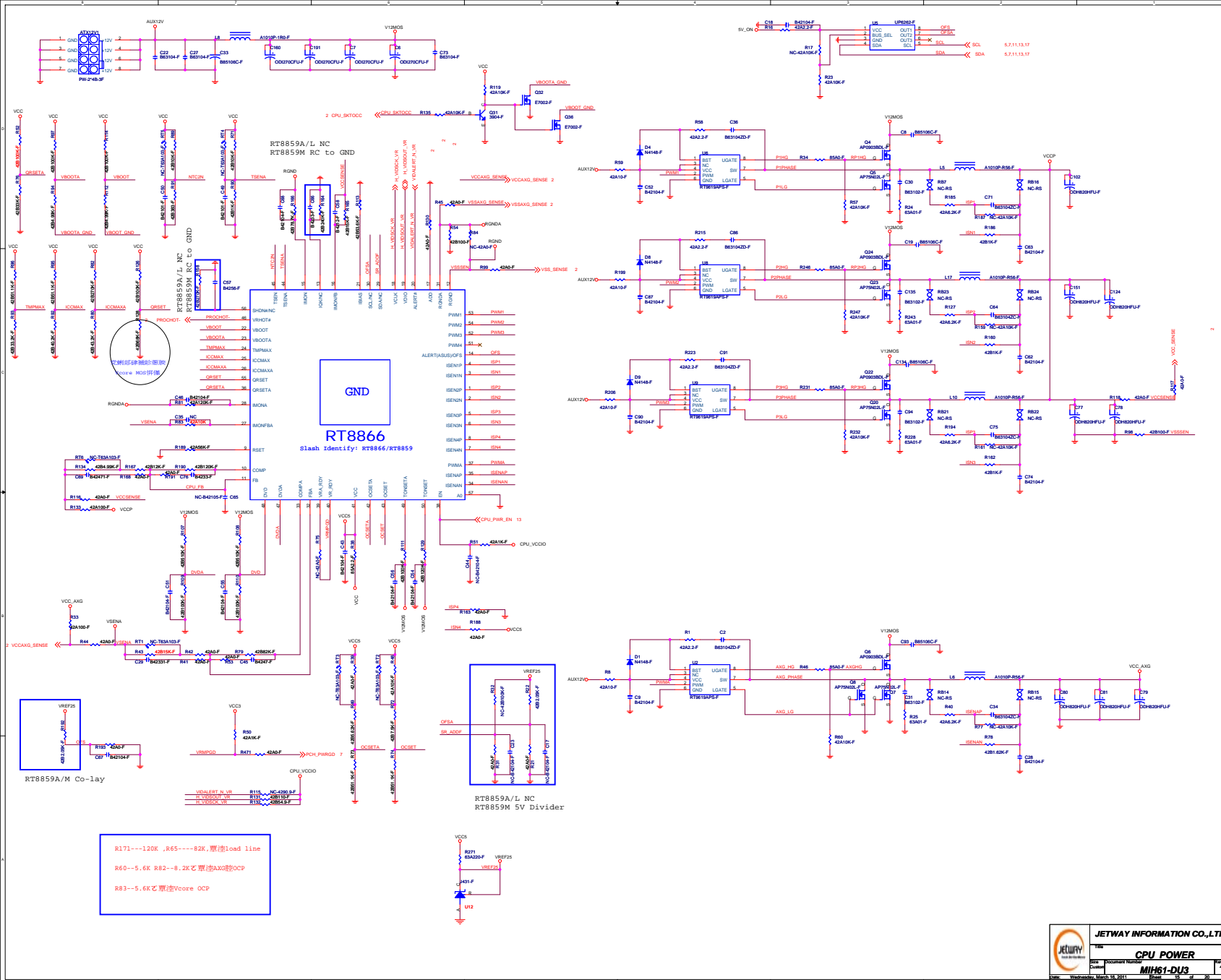




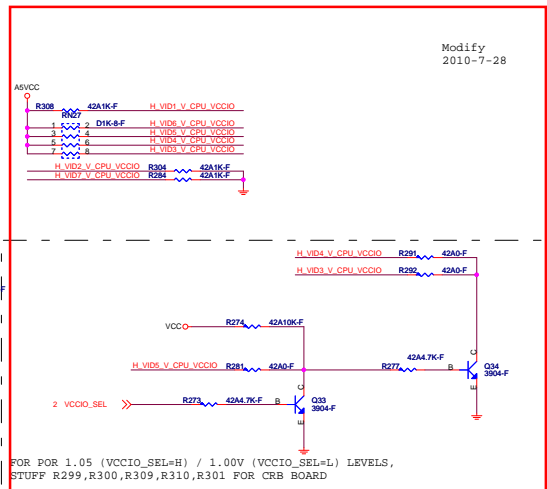
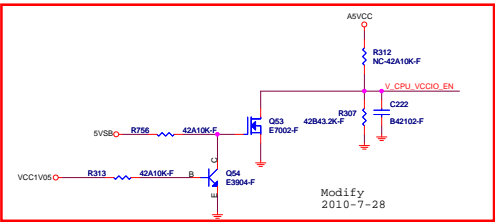
\*\* Terminate ground plane as close to power supply as possible.  
Digital Gnd      Analog Gnd



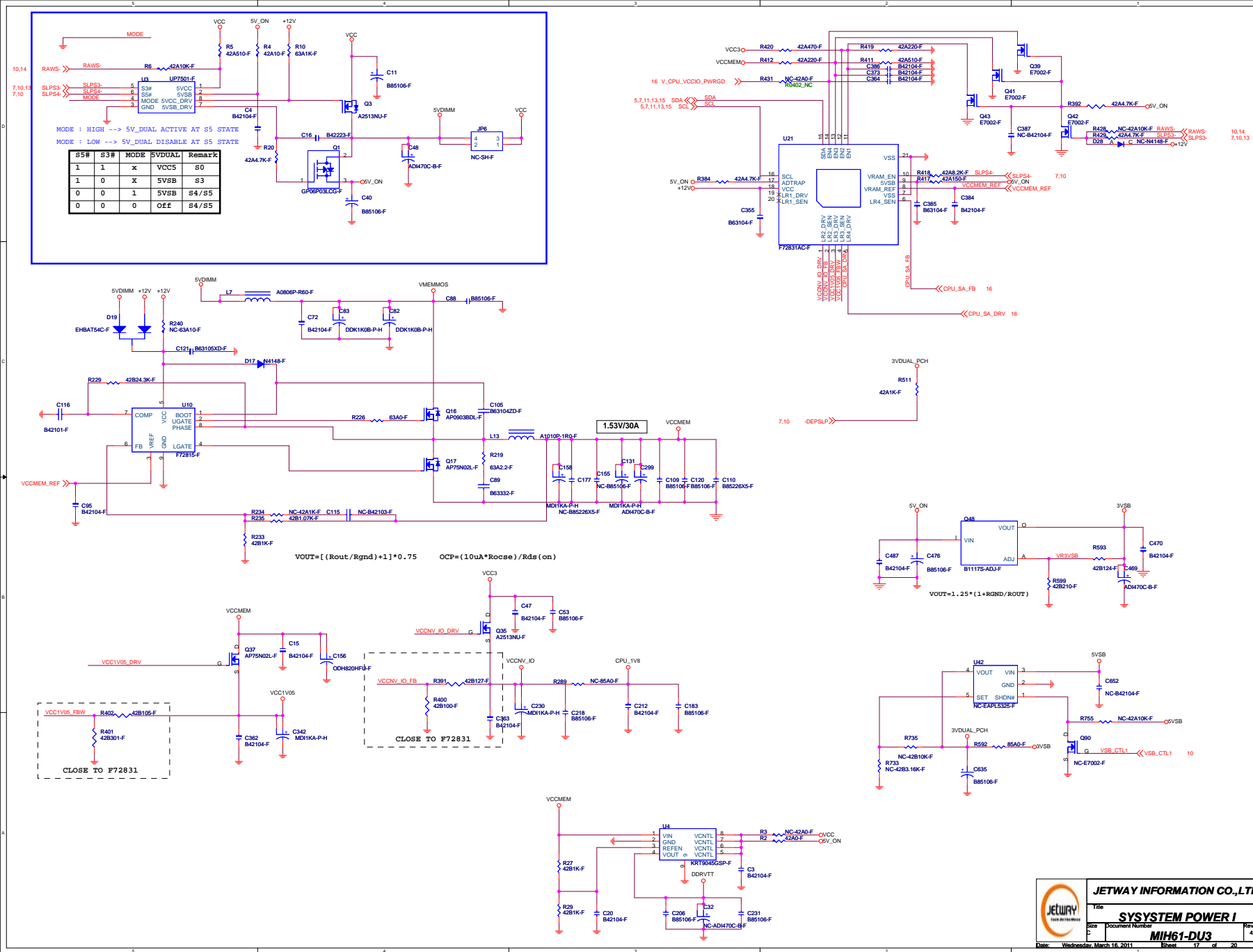




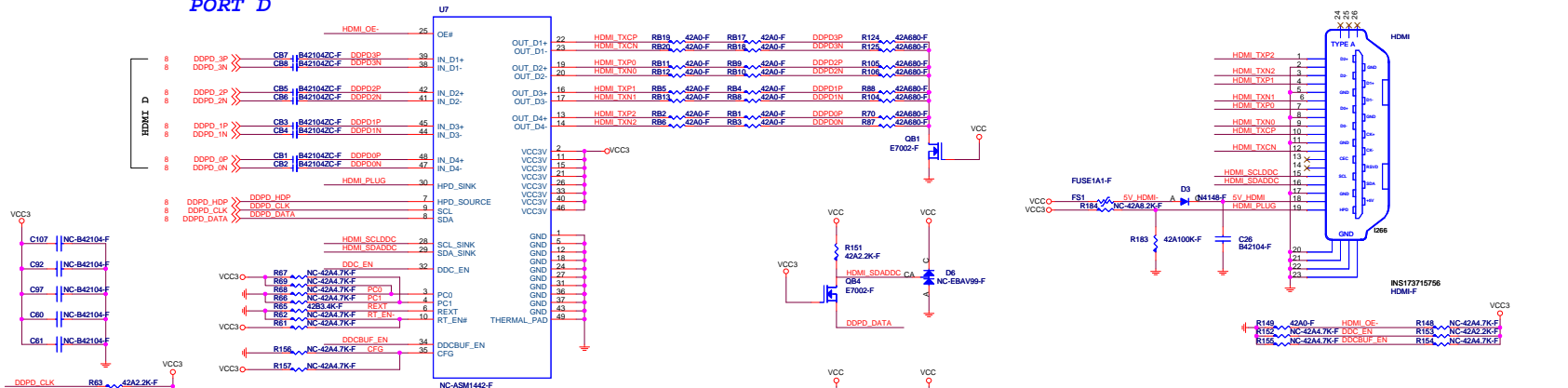




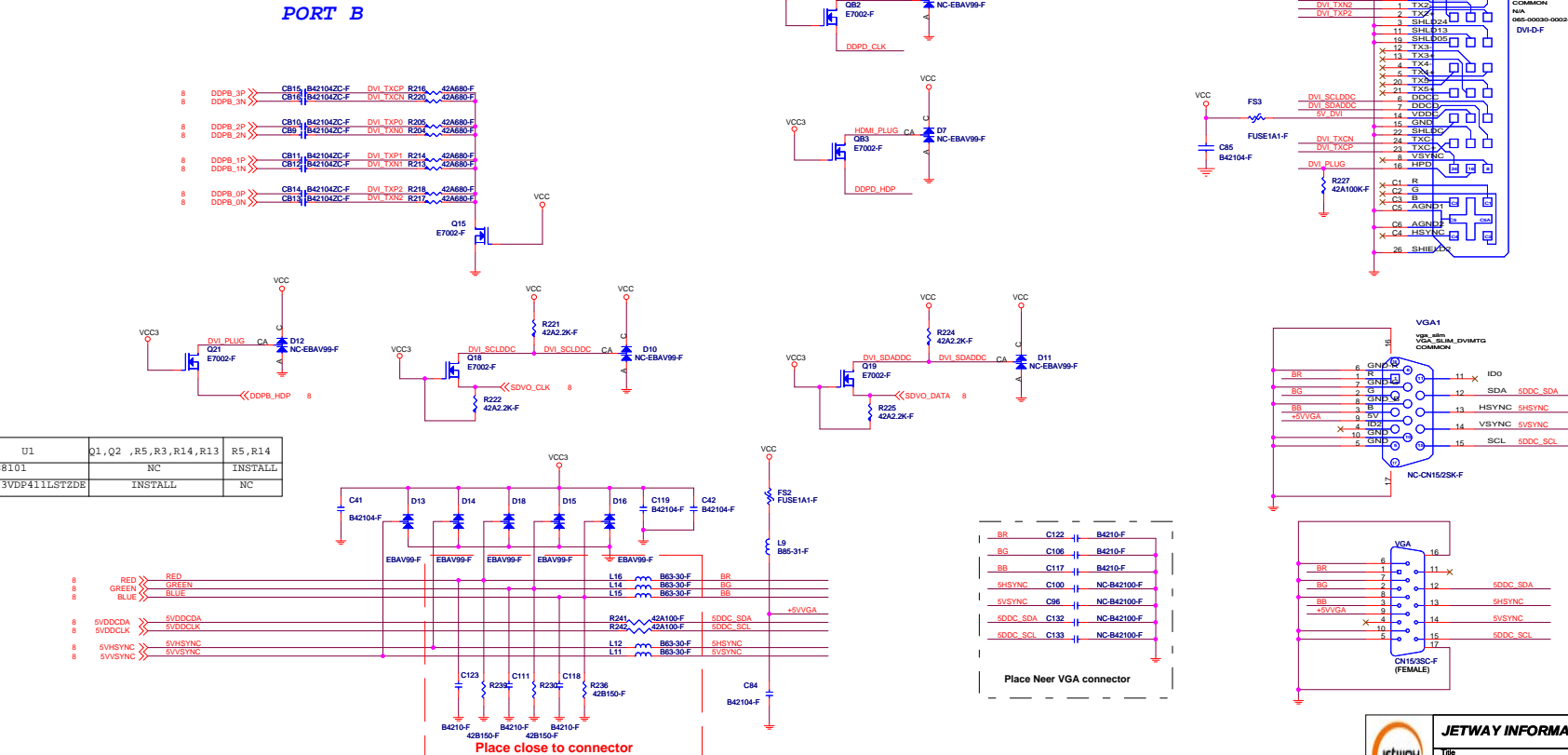
Modify  
2010-7-28



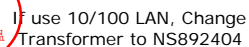
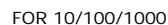
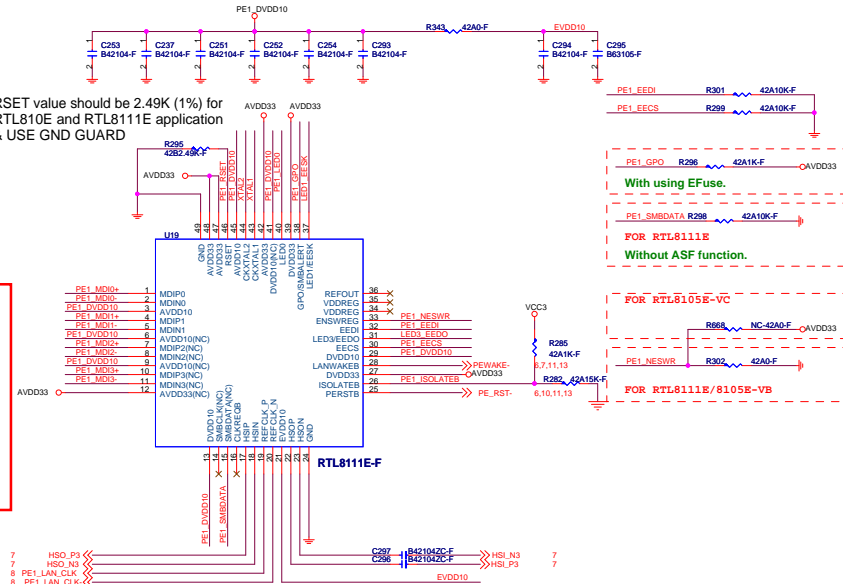
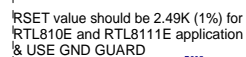
## PORT D

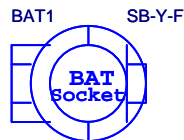


## PORT B



U1	Q1,Q2 ,R5,R3,R14,R13	R5,R14
PS8101	NC	INSTALL
PT3VDP411LSTZDE	INSTALL	NC





**BATTERY HOLDER** 無鉛製程

**IH65R00**



**IH65R00 30.5\*24.5cm PCB**

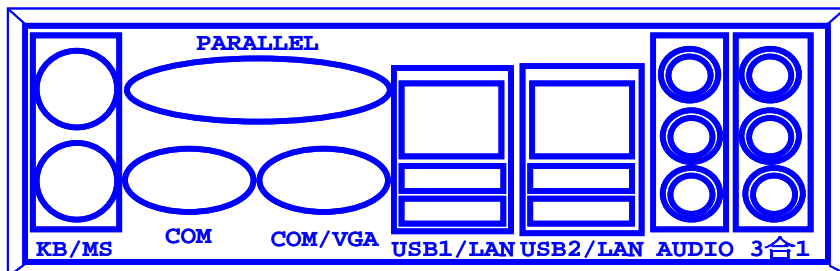
JP1(1-2)1  
SPYE-F



SHUNT  
JUMPER

**JUMPER YELLOW** 無鉛製程

**背板鐵片1 098-3-F**



**F04-104 改Audio右三孔半破**



**JETWAY INFORMATION CO.,LTD.**

Title

**ACCESSORY**

Size  
A

Document Number

**MIH61-DU3**

Rev  
3.0

Date: Wednesday, March 16, 2011

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